## REMARKS

Claims 1-15 are present in this application. Claims 1, 3, 5, and 8 are currently independent.

### Allowed Claims

Applicant thanks the Examiner for indicating that claims 3, 4, 6, 7, 9, and 12 are allowed.

### Claim Rejection – 35 USC 102

Claims 1, 2, 5, 8, 10, 11, 13, and 14 have been rejected under 35 U.S.C. 102(e) as being anticipated by Tajima et al. (U.S. Patent 6,373,911). Applicant respectfully traverses this rejection.

Claim 1 (e.g., Figure 8) is directed to a bit synchronizing circuit comprising a detection circuit for detecting which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation circuit with respect to one of the generated clocks, and a clock selecting circuit having two inputs, one from the polyphase clock generation circuit and a detection result from the detection circuit, and produces one output, a selected polyphase clock.

The Office Action states that, "The input data signal [of Tajima] having timing information is interpreted as the input clock signal." In

other words, the Office Action indicates that the data input signal of Tajima has timing information, and therefore can be considered an "input clock".

In order to clarify what was intended by the claimed "input clock," claim 1 has been amended to recite that the "input clock" input to the detection circuit is "one of the plurality of generated clocks: generated by the polyphase clock generation circuit. In a preferred embodiment of the present invention, the input clock is, for example, generated as "CLOCK 0." Tajima's data input, on the other hand, is not generated by the multi-phase clock generator circuit 2.

Applicant submits that Tajima fails to teach at least the claimed detection circuit for detecting which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation circuit with respect to one of the plurality of generated clocks.

Further, with respect to claim 5, the Office Action states that the function of the operational circuit can be interpreted as "providing center position by averaging a plurality of outputs from the detection circuit, which is equivalent to the operation of the determining circuit," (relying on Tajima at column 3, lines 1-3). The Office Action further states that,

the operation carried out on the average of the Tajima's determining means is to hold it for a period of time by the holding circuit.

Tajima at column 2, line 66, to column 3, line 3, states,

"phase determining means for determining the clock occurring level transition timing at substantially center portion of mutually adjacent level transition timings of the input data depending upon a plurality of phase comparison outputs of the phase comparator means."

Applicant submits that while Tajima does appear to teach performing an operation then holding the result of the operation, the operational circuit of the present invention samples an output from the detection circuit a plurality of times and carries out an operation on the sampled values.

The present specification expresses that the embodiment of Fig. 6, for example, "samples the outputs from the detection circuit 610 a plurality of times ... and performs an operation at the sampling/operational circuit 620 so as to take a mean value of the sampled values." (page 22, lines 3-8). In other words, unlike Tajima, the present invention samples the outputs from the detection circuit (e.g., phase comparison circuit 4) a plurality of times and performs an operation on the plurality of sampled values.

Thus, while Tajima may teach performing an operation, the present invention samples values a plurality of times before performing an operation on the sampled values. In order to clarify the operation performed in the claimed operational circuit claim 5 has been amended to recite the function "carrying out an operation on the plurality of sampled values."

Thus, at least for this reason, as well as reasons set forth above for claim 1, Applicant submits that Tajima fails to teach at least the claimed operational circuit for sampling an output from the detection circuit a plurality of times and carrying out an operation on the plurality of sampled values.

Further, with respect to claim 8, the Office Action generally states that Tajima's flip-flops 401 to 404 meet a definition of "bit synchronous working circuits", as being "a type of digital circuit configured to perform a predetermined operation on a signal synchronously." Applicant respectfully disagrees.

Applicant submits that even if it could be said that flip-flops of Tajima are digital circuits that operate synchronously, which Applicant does not concede, the flip-flops do not carry out a "bit synchronizing operation," as recited in the claim.

Furthermore, claim 8, similar to the above for claim 1, has been amended to clarify the intended meaning of "the input clock" to that of "one of said plurality of generated clocks."

Thus, at least for this reason, as well as the reasons set forth above for claim 1, Applicant submits that Tajima fails to teach each and every element of claim 8.

The same argument applies as well to the respective dependent claims. Accordingly, Applicant respectively requests that the rejection be withdrawn.

**CONCLUSION**

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the present application is in condition for allowance and such allowance is respectfully solicited. Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert W. Downs (Reg. No. 48,222), to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any

overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1. 17; particularly, extension of time fees.

Respectfully submitted,

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